Amendments to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of Claims:

1-34. (Cancelled)

35. (Currently Amended) A method for jitter compensation in a phase locked loop frequency synthesizer, the method comprising the step of:

compensating for the jitter prior to passing a signal subject to jitter through a non-linearity, said compensating comprising a variable delay realized by means of a tapped delay line;

wherein each of a plurality of integer divisors are selected according to a fractional pattern, representing fractional weighting of the integer divisors, generated by a ΣΔ modulator from a fractional setting input.

36. (Cancelled).

37. (Previously Presented) The method according to claim 35, wherein a fraction of a first and a second integer is determined by a binary fractional pattern, for selecting the first or the second integer, generated by a ΣΔ modulator from a fractional setting input.

38. (Currently Amended) The method according to claim [[36]] 35, wherein the tapped delay line is controlled by means of control signals derived from the ΣΔ modulator.

39. (Previously Presented) The method according to claim 38, wherein a control signal for controlling the tapped delay line is determined by integrating and scaling an error signal being the difference between a signal representing the fraction and a signal carrying the fractional pattern.

40. (Previously Presented) The method according to claim 35, wherein the tapped delay line comprises a plurality of capacitors with capacitances proportional to successive powers of 2.

41. (Previously Presented) The method according to claim 39, wherein the control signal carries a binary number whose bit representation connects or disconnects capacitors of the tapped delay line with respective capacitances corresponding to bit positions of the binary representation.

42. (Previously Presented) The method according to claim 35, wherein the tapped delay line comprises a plurality of serially connected delay elements.

43. (Previously Presented) The method according to claim 39, wherein the control signal carries a representation for connecting or disconnecting a delay element of the tapped delay line to either the input or output of the tapped delay line.

44. (Previously Presented) The method according to claim 43, wherein the control signal carries a bit representation for connecting or disconnecting a delay element output to the output of the tapped delay line.

45. (Previously Presented) The method according to claim 43, wherein the control signal carries a bit representation for connecting or disconnecting a delay element input to the input of the tapped delay line.

46. (Previously Presented) The method according to claim 35, wherein the non-linearity is included in or is a phase or frequency detector.

47. (Previously Presented) The method according to claim 35, wherein the output signal of the tapped delay line is input to the phase or frequency detector.

48. (Previously Presented) The method according to claim 35, wherein at least one of a reference frequency signal, a frequency divided output signal of a voltage controlled oscillator, or a frequency divided output signal of the frequency synthesizer is input to and delayed by the tapped delay line.

49. (Previously Presented) The method according to claim 35, wherein the output signal of the tapped delay line is input to frequency dividing circuitry.

50. (Previously Presented) The method according to claim 35, wherein at least one of an output signal of a voltage controlled oscillator and an output signal of the frequency synthesizer is input to and delayed by the tapped delay line.

51. (Currently Amended) A phase locked loop frequency synthesizer with jitter compensation, the frequency synthesizer comprising:

a tapped delay line for compensating the jitter prior to passing a signal subject to jitter through a non-linearity; and,

a ΣΔ modulator for generating, or a storing element for pre-generated storing, of a fractional pattern representing fractional weighting of a plurality of integer divisors, wherein the fractional pattern identifies one integer divisor, out of the plurality of integer divisors, at a time to be active.

52. (Cancelled).

53. (Previously Presented) The frequency synthesizer according to claim 51, comprising a ΣΔ modulator for generating or a storing element for pre-generated storing of a binary fractional pattern for determining a fraction of a first and a second integer, the binary fractional pattern selecting the first or the second integer, the binary fractional pattern being generated from or restored from a fractional setting input.

54. (Previously Presented) The frequency synthesizer according to claim 53, comprising control means for controlling the tapped delay line by means of one or more control signals derived from the ΣΔ modulator.

55. (Previously Presented) The frequency synthesizer according to claim 54, comprising an integrator for integrating and scaling an error signal being the difference between a signal representing the fraction and a signal carrying the binary fractional pattern, the integrator output signal being a signal for controlling the tapped delay line.

56. (Previously Presented) The frequency synthesizer according to claim 51, wherein the tapped delay line comprises a plurality of capacitors with capacitances proportional to successive powers of 2.

57. (Previously Presented) The frequency synthesizer according to claim 55, comprising switches for connecting or disconnecting capacitors of the tapped delay line, wherein respective capacitances corresponding to bit positions of a binary representation of a binary number are connected or disconnected, the binary number being carried by the one or more control signals.

58. (Previously Presented) The frequency synthesizer according to claim 51, wherein the tapped delay line comprises a plurality of serially connected delay elements.

59. (Previously Presented) The frequency synthesizer according to claim 55, comprising one or more switches for connecting or disconnecting one or more delay elements to the input or output of the tapped delay line according to a bit representation, the bit representation being carried by a control signal.

60. (Previously Presented) The frequency synthesizer according to claim 59, wherein the one or more switches each connects or disconnects a delay element output to the output of the tapped delay line.

61. (Previously Presented) The frequency synthesizer according to claim 59, wherein the one or more switches each connects or disconnects a delay element input to the input of the tapped delay line.

62. (Previously Presented) The frequency synthesizer according to claim 51, wherein the non-linearity is included in or is a phase or frequency detector.

63. (Previously Presented) The frequency synthesizer according to claim 51, wherein the output signal of the tapped delay line is input to the phase or frequency detector.

64. (Previously Presented) The frequency synthesizer according to claim 51, wherein at least one of a reference frequency signal, a frequency divided output signal of a voltage controlled oscillator, and a frequency divided output signal of the frequency synthesizer is input to and delayed by the tapped delay line.

65. (Previously Presented) The frequency synthesizer according to claim 51, wherein the output signal of the tapped delay line is input to frequency dividing circuitry.

66. (Previously Presented) The frequency synthesizer according to claim 51, wherein at least one of an output signal of a voltage controlled oscillator and an output signal of the frequency synthesizer is input to and delayed by the tapped delay line.

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